Reference Specification

for connection of

Call Switching Equipment

with

2048 kbit/s Digital Interface

to the

Public Switched Telephone Network (PSTN)

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PART A INTRODUCTION

1 SCOPE

1.1 The technical requirements identify the minimum requirements for the connection of call switching equipment with 2048 kbit/s interface to the Public Switched Telephone Network (PSTN).

1.2 The contents in **PART B** cover the physical and electrical characteristics for the 2048 kbit/s interface necessary for the transmission and reception of signals in digital form (based on ITU-T Recommendation G.703 § 6). For signals with bit rates of n x 64 kbit/s (n = 2 to 31) which are routed through multiplexing equipment specified for 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface described in Part B.

1.3 The contents in **PART § 2** (based on ITU-T Recommendation G.704 § 2.3) give the functional characteristics of the basic frame structures used at the 2048 kbit/s interface, including frame length, frame alignment signals, and cyclic redundancy check (CRC) procedures. Information on how channels at 64 kbit/s and n x 64 kbit/s are accommodated within the basic frame structures is provided in **PART C § 3** (based on ITU-T Recommendation G.704 § 5).

1.4 Specific requirements for call switching equipment covering PABX signalling scheme and other protocols, are not included in this Specification. Technical Requirements for Channel Associated Signalling (CAS) and Common Channel Signalling schemes are contained in separate Specifications.

NOTE - Divergence from ITU-T Recommendations will be shown by the addition of texts (in italic) or the deletion of texts (through strikeouts).

2 GENERAL REQUIREMENTS

2.1 POWER SUPPLY

Call Switching Equipment may be a.c. powered or d.c. powered. For an a.c. powered equipment, the technical requirements shall be complied with when operating from an a.c. mains supply of voltage, 230V ± 10% and frequency, 50 Hz ± 2%. Where external power supply is used, e.g. AC adaptor, it shall not affect the capability of the equipment to meet the technical requirements.

2.2 IDENTIFICATION OF EQUIPMENT

The equipment shall be marked with the supplier's or manufacturer's name or identification mark, and the supplier's or manufacturer's model or type reference. The markings required shall be legible, indelible and readily visible.

3	SAFETY OF TERMINAL EQUIPMENT FOR CONNECTION TO TELECOMMUNICATION NETWORKS	CR
3.1	**General**	–
3.1.1	Equipment (mains or battery powered) shall be designed to comply with the principles of Singapore Standards (SS), International Electrotechnical Commission (IEC) or other safety standards e.g. IEC 60950, EN60950, BS EN41003, SS 337. Requirements applicable to the equipment (e.g. class of equipment, type of TNV circuit and types of components) covered in the following sections of IEC 60950[1] shall be identified and complied with: Scope (1.1 of IEC 60950) Definitions (1.2 of IEC 60950) General requirements (1.3 of IEC 60950) General conditions for test (1.4 of IEC 60950) Components (1.5 of IEC 60950) Power interface (1.6 of IEC 60950) Marking and instructions (1.7 of IEC 60950) Protection from hazards (2 of IEC 60950) Wiring, connections and supply (3 of IEC 60950) Physical requirements (4 of IEC 60950) Thermal and electrical requirements (5 of IEC 60950) Connection to telecommunication networks (6 of IEC 60950)	M
3.2	**TNV[2] circuit characteristics and requirements**	–
3.2.1	In a single TNV circuit or interconnected TNV circuits, the voltage between any two conductors of the TNV circuit or circuits and between any one such conductor and earth shall comply with the limits set for TNV-1[3] circuit (refer to 6.2.1.1 (a) of IEC 60950).	M
3.2.2	Requirements for separation from other circuits and from accessible parts are in accordance with Table 19 of 6.2.1.2, IEC 60950.	M
3.2.3	The equipment shall be able to withstand the operating voltages generated externally as described in 6.2.1.3 of IEC 60950.	M
3.2.4	TNV circuits shall be separated from circuits at hazardous voltages by one or both of the methods given in 6.2.1.4 of IEC 60950.	M
3.2.5	If the TNV circuit is connected to other circuits, the requirements as given in 6.2.1.5 of IEC 60950 shall be complied with.	Note 1

[1] IEC 60950, 2nd Edition, 1991 + Amend. 1, 1992 + Amend. 2, 1993 + Amend. 3, 1995 + Amend. 4, 1996

[2] Telecommunication Network Voltage (TNV) as defined in 1.2.8.8, IEC 60950 Amend. 4, 1996

[3] Only TNV-1 circuits are permitted for connection to the Singapore telecommunication network. Operating voltages of TNV-1 circuits do not exceed 42.4 V peak or 60 V d.c. under normal operating conditions ((refer to 1.2.8.9 and 2.3.2 of IEC 60950 Amend. 4, 1996).

3	**SAFETY OF TERMINAL EQUIPMENT FOR CONNECTION TO TELECOMMUNICATION NETWORKS** (Continued)	**CR**
3.3	**Protection of telecommunication network service personnel, and users of other equipment connected to the network, from hazards in the equipment**	–
3.3.1	Circuitry intended to be directly connected to a telecommunication network shall comply with the requirements for an SELV[4] circuit or a TNV-1 circuit (refer to 6.3.1 of IEC 60950).	M
3.3.2	Where protection of telecommunication network relies on the protective earthing of the equipment, the equipment installations instructions and other relevant literature shall state that integrity of protective earthing must be ensured (refer to 6.3.2 of IEC 60950).	Note 2
3.3.3	There shall be insulation between circuitry intended to be connected to a telecommunication network and any parts or circuitry that will be earthed (refer to 6.3.3 of IEC 60950).	M
3.3.4	The leakage current to a telecommunication network originating from a mains powered equipment shall not exceed 0.25 mA r.m.s. (refer to 6.3.4.1 of IEC 60950). This requirement does not apply to equipment where the circuit to be connected to a telecommunication network is connected to an earthing terminal in the equipment.	Note 2
3.4	**Protection of equipment users from over voltages on telecommunication networks**	–
3.4.1	Equipment shall provide adequate electrical separation between TNV-1 circuit and certain parts of the equipment (refer to 6.4.1 of IEC 60950).	M
3.4.2	Compliance with 3.4.1 is checked by the electric strength test procedure of 6.4.2 of IEC 60950.	M
3.5	**Protection of the telecommunication wiring system from overheating**	–
3.5.1	Equipment intended to provide power over the telecommunication wiring system to remote equipment shall limit the output current to a value that does not cause damage to the telecommunication wiring system (refer to 6.5 of IEC 60950).	Note 2
Note 1	Requirements are mandatory if TNV circuits are connected to other circuits.	
Note 2	Requirements are mandatory if clause is applicable.	

[4] Safety Extra Low Voltage (SELV) circuit is so designed and protected that under normal and single fault conditions, its voltages do not exceed a safe value of 42.4 V peak or 60 Vd.c. under normal operating conditions.

PART B PHYSICAL / ELECTRICAL CHARACTERISTICS OF HIERARCHICAL DIGITAL INTERFACES

1 GENERAL
(ITU-T Recommendation G.703 1991)

The ITU-T,

considering

that interface specifications are necessary to enable the interconnection of digital network components (digital sections, multiplex equipment, exchanges) to form an international digital link or connection;

that Recommendation G.702 defines the hierarchical levels;

that Recommendation G.704 deals with the functional characteristics of interfaces associated with network nodes;

that I.430 series Recommendations deal with the layer 1 characteristics for ISDN user-network interfaces;

recommends

that physical and electrical characteristics of the interfaces at hierarchical bit rates should be as described in this Recommendation.

Note 1 - The characteristics of interfaces at non-hierarchical bit rates, except n x 64 kbit/s interfaces conveyed by 2048 kbit/s interfaces, are specified in the respective equipment Recommendations.

Note 2 - The jitter specifications contained in the following § 2 are intended to be imposed at international interconnection points.

Note 3 - The interface described in § 2 corresponds to the port T (output port) and T' (input port) recommended for interconnection in ITU-R Recommendation AC/9 with reference to Report AH/9 of ITU-R Study Group 9. (This Report defines the points T and T'.)

Note 4 - For signals with bit rates of n x 64 kbit/s (n = 2 to 31) which are routed through multiplexing equipment specified for the 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface specified in § 2.

2 INTERFACE AT 2048 kbit/s
(ITU-T Recommendation G.703 § 6 1991)

2.1 GENERAL CHARACTERISTICS

The call switching equipment shall conform with the relevant parts of ITU-T Recommendations G.703 and G.823 which refer to a digital interface operating at 2048 kbit/s.

Bit rate : 2048 kbit/s ± 50 ppm

Code : HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement : see Annex B.

Timing : The interface timing arrangements are co-directional. The call switching equipment shall synchronise its bit timing to the signal received from the network. In the event of loss of received signal the call switching equipment shall derive its output timing from its internal clock.

2.2 SPECIFICATIONS AT THE OUTPUT PORTS

Table 2.1 : Output port characteristics (Table 6/G.703)

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask as shown in ITU-T Rec figure 15/G.703 irrespective of the sign.	
Pair(s) in each direction	~~One coaxial pair (see § 2.4)~~	One symmetrical pair (see § 2.4)
Test load impedance	~~75 Ω resistive~~	120 Ω resistive
Nominal peak voltage of a mark (pulse)	~~2.37 V~~	3 V
Peak voltage of a space (no pulse)	~~0 ± 0.237 V~~	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at an output port	Refer to § 2 of ITU-T Rec G.823	

2.3 SPECIFICATIONS AT THE INPUT PORTS

2.3.1 The digital signal presented at the input port shall be as defined for the output port but modified by the characteristics of the interconnecting pair. The attenuation of this pair shall be assumed to follow *Öf* law and the loss at a frequency of 1024 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipment.

2.3.2 For jitter to be tolerated at the input port, refer to § 3 of ITU-T Rec G.823.

2.3.3 The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
51 to 102	12
102 to 2048	18
2048 to 3072	14

2.3.4 To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate *of 2048 kbit/s*, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance of ~~75 ohms (in the case of coaxial-pair interface) or~~ 120 ohms (in the case of symmetrical-pair interface), to give a signal-to-interference ratio of 18 dB. The binary content of the interfering signal should comply with ITU-T Rec O.151 (2^{15} - 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

Note - A receiver implementation providing an adaptive rather than a fixed threshold is considered to be robust against reflections and should be therefore be preferred.

2.4 EARTHING OF ~~OUTER CONDUCTOR OR~~ SCREEN

The ~~outer conductor of the coaxial pair or the~~ screen of the symmetrical pair shall be connected to earth at the output port and provision shall be made for connecting ~~the outer conductor of the coaxial pair or~~ the screen of the symmetrical pair to earth if required, at the input port.

ANNEX A

(to Recommendation G.703)

DEFINITION OF CODES

This annex defines the modified alternate mark inversion codes (see Recommendation G.701, item 9005) whose use is specified in this Recommendation.

In these codes, binary 1 bits are generally represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions, as specified for the individual codes, are made when strings of successive 0 bits occur in the binary signal.

In the definitions below, B represents an inserted pulse conforming to the AMI rule (Rec. G.701, 9004), and V represents an AMI violation (Rec. G.701, 9007).

The encoding of binary signals in accordance with the rules given in this annex includes frame alignment bits, etc.

A.1 Definition of B3ZS (also designated HDB2) and HDB3

Each block of 3 (or 4) successive zeros is replaced by 00V (or 000V respectively) or B0V (B00V). The choice of 00V (000V) or B0V (B00V) is made so that the number of B pulses between consecutive pulses V is odd. In other words, successive V pulses are of alternate polarity so that no d.c. component is introduced.

Note - The abbreviations stand for the following:

HDB2 (HDB3)	high density bipolar of order 2 (3)
B3ZS	bipolar with three-zero substitution.

A.2 Definition of B6ZS and B8ZS

Each block of 6 (or 8) successive zeros is replaced by 0VB0VB (or 000VB0VB respectively).

ANNEX B

(to Recommendation G.703)

SPECIFICATION OF THE OVERVOLTAGE PROTECTION REQUIREMENT

The input and output ports should withstand without damage the following tests:

- 10 standard lightning impulses (1.2/50 µs) with a maximum amplitude of U (5 negative and 5 positive impulses). For the definition of this impulse see Ref. [1].

- at the interface for coaxial pairs:

  i) differential mode: with a pulse generator of Figure B-l/G.703, the value of U is under study;
  ii) common mode - under study;

- at the interface for symmetrical pairs:
  i) differential mode: with a pulse generator of Figure B-l/G.703, the value of U is under study (a value of 20 V has been mentioned);
  ii) common mode: with a pulse generator of Figure B-2/G.703, U = 100 V_{dc}.

Possible pulse generators are described in Figures B-l/G.703 and B-2/G.703.

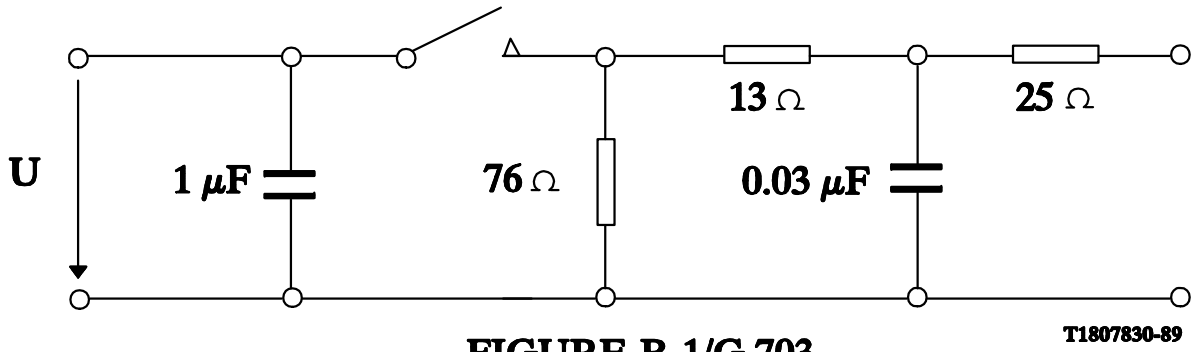

FIGURE B-1/G.703

Pulse generator 1.2/50 µs for differential mode voltages

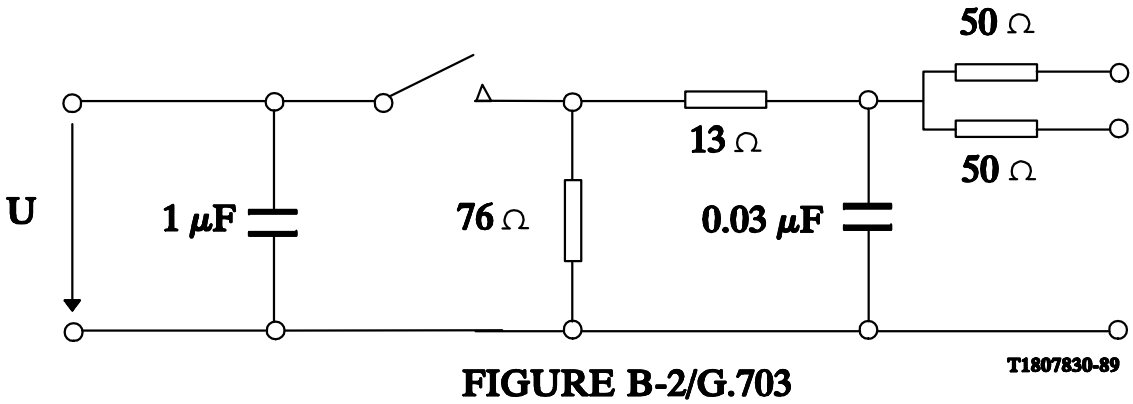

FIGURE B-2/G.703

Pulse generator 1.2/50 μs for common mode voltages at symmetrical interfaces

References

{1} IEC publication No. 60-2 High-voltage test techniques, Part 2: Test procedures, Geneva, 1973.

ANNEX C

(to Recommendation G.703)

ALPHABETICAL LIST OF ABBREVIATIONS USED IN THIS RECOMMENDATION

AIS	Alarm indication of signal
B3ZS	Bipolar with three-zero substitution
CMI	Coded mark inversion
HDB2	High density bipolar of order 2 code
HDB3	High density bipolar of order 3 code

PART C SYNCHRONOUS FRAME STRUCTURES USED AT PRIMARY AND SECONDARY HIERARCHICAL LEVELS

1 SCOPE
(ITU-T Recommendation G.704 § 1 Mar 1994)

This Recommendation gives functional characteristics of interfaces associated with:

- network nodes, in particular, synchronous digital multiplex equipment and digital exchanges in IDNs for telephony and ISDNs, and

- PCM multiplexing equipment.

Section 2 deals with basic frame structure, including details of frame length, frame alignment signals, cyclic redundancy check (CRC) procedures and other basic information.

Section 3 contains more specific information about how certain channels at 64 kbit/s and at other bit rates are accommodated within the basic frame structures described in § 2.

Electrical characteristics for these interfaces are defined in Recommendation G.703.

Note 1- This Recommendation does not necessarily apply to those cases where the signals that cross the interfaces are devoted to non-switched connections, such as those for the transport of encoded wideband signals (e.g. broadcast TV signals or multiplexed sound-program signals which need not be individually routed via the ISDN), see also Annex A to Recommendation G.702.

Note 2 -The frame structures recommended in this Recommendation do not apply to certain maintenance signals, such as the all 1s signals transmitted during fault conditions or other signals transmitted during out-of-service conditions.

Note 3 - Frame structures associated with digital multiplexing equipments using justification are covered in each corresponding equipment Recommendation.

Note 4 - Inclusion of channel structures at other bit rates than 64 kbit/s is a matter for further study Recommendations G.761 and G.763 dealing with the characteristics of PCM/ADPCM transcoding equipment contain information about channel structures at 32 kbit/s. The more general use of those particular structures is a subject of further study.

2 BASIC FRAME STRUCTURE AT 2048 kbit/s (ITU-T Recommendation G.704 § 2.3 Mar 1994)

2.1 FRAME LENGTH

256 bits, numbered 1 to 256. The frame repetition rate is 8000 Hz.

2.2 ALLOCATION OF BITS NUMBER 1 TO 8 OF THE FRAME

Allocation of bits number 1 to 8 of the frame is shown in Table 2.1.

Table 2.1 : Allocation of bits 1 to 8 of the frame (Table 5a/G.704)

Bit number / Alternate frames	1	2	3	4	5	6	7	8
Frame containing the frame alignment signal	S_i	0	0	1	1	0	1	1
	Note 1	Frame alignment signal						
Frame not containing the frame alignment signal	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note 1	Note 2	Note 3	Note 4				

Note 1 - S_i = bits reserved for international use. One specific use is described in § 2.3. Other possible uses may be defined at a later stage. If no use is realised, these bits should be fixed at 1 on digital paths crossing an international border. However, they may be used nationally if the digital path does not cross a border.

Note 2 - This bit is fixed at 1 to assist in avoiding simulations of the frame alignment signal.

Note 3 - A = Remote alarm indication. In undisturbed operation, set to 0; in alarm condition, set to 1.

Note 4 - S_{a4} to S_{a8} = Additional spare bits whose use may be as follows:

i) Bits S_{a4} to S_{a8} may be recommended by ITU-T for use in specific point-to-point applications (e.g. transcoder equipment conforming to ITU-T Rec G.761).

ii) Bit S_{a4} may be used as a message-based data link to be recommended by ITU-T for operations, maintenance and performance monitoring. This channel originates at the point where the frame is generated and terminates where the frame is split up. This requires further study;

iii) Bits S_{a4} to S_{a7} are for national usage where there is no demand on them for specific point-to-point applications, [see i) above].

Bits S_{a4} to S_{a8} (where these are not used) should be set to 1 on links crossing an international border.

2.3 DESCRIPTION OF THE CRC-4 PROCEDURE IN BIT 1 OF THE FRAME

2.3.1 Special use of bit 1 of the frame

Where there is a need to provide additional protection against simulation of the frame alignment signal and/or where there is a need for an enhanced error monitoring capability, then bit 1 should be used for a cyclic redundancy check-4 (CRC-4) procedure as detailed below.

Note - Equipment incorporating the CRC-4 procedure should be designed to be capable of interworking with equipment which does not incorporate the CRC-4 procedure, that is, an ability to continue to provide service (traffic) between equipment with and without a CRC-4 capability. This can be achieved either manually (e.g. by straps) or automatically.

- For the manual case, the equipment incorporating the CRC-4 procedure should be capable of fixing bit 1 of the frame to the binary "1" state (see Table 2.1, Note 1).

- For automatic case, this can be achieved at the equipment having the CRC-4 capability either:

- as a "higher-layer" function under the control of a network management facility (e.g. a TMN) - the details are for further study; or

- as a "lower-layer" function using a modified CRC-4 multiframe alignment algorithm as described in Annex B of ITU-T Rec G.706.

2.3.2 The allocation of bits 1 to 8 of the frame is shown in Table 2.2 for a complete CRC-4 multiframe.

Table 2.2 : CRC-4 multiframe structure (Table 5b / G.704)

	Sub - multiframe (SMF)	Frame number	Bits 1 to 8 of the frame							
			1	2	3	4	5	6	7	8
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

Note 1 - E = CRC-4 error indication bits (see § 2.3.4)

Note 2 - S_{a4} to S_{a8} = Spare bits (see Note 4 to Table 2.1)

Note 3 - C_1 to C_4 = Cyclic redundancy check-4 (CRC-4) bits (see § 2.3.4 and 2.3.5)

Note 4 - A = Remote alarm indication (see Table 2.1)

2.3.3 Each CRC-4 multiframe, which is composed of 16 frames numbered 0 to 15, is divided into two 8-frame sub-multiframes (SMF), designated SMF I and SMF II which signifies their respective order of occurrence within the CRC-4 multiframe structure. The SMF is the cyclic redundancy check-4 (CRC-4) block size (i.e. 2048 bits).

The CRC-4 multiframe structure is not related to the possible use of a multiframe structure in 64 kbit/s channel time slot 16 (see § 3.1.3.2).

2.3.4 Use of bit 1 in 2048 kbit/s CRC-4 multiframe

In those frames containing the frame alignment signal (defined in § 2.2), bit 1 is used to transmit the CRC-4 bits. There are four CRC-4 bits, designated C1, C2, C3 and C4 in each SMF.

In those frames not containing the frame alignment signal (see § 2.2), bit 1 is used to transmit the 6-bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E).

The CRC-4 multiframe alignment signal has the form 001011.

The E-bits should be set to "0" until both basic frame and CRC-4 multiframe alignment are established (see ITU-T Rec G.706, § 4). Thereafter, the E-bits should be used to indicate received errored sub-multiframes by setting the binary state of one E-bit from 1 to 0 for each errored sub-multiframe. Any delay between the detection of an errored sub-multiframe and the setting of the E-bit that indicates the error state must be less than 1 second.

Note 1 - The E-bits will always be taken into account even if the SMF which contains them is found to be

errored, since there is little likelihood that the E-bits themselves will be errored.

Note 2 - In the short term, there may exist equipment which do not use the E-bits; in this case the E-bits are set to binary 1.

2.3.5 Cyclic redundancy check (CRC)

2.3.5.1 Multiplication/division process

A particular CRC-4 word, located in sub-multiframe N, is the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of sub-multiframe N- 1).

Note 1 - When representing the contents of the check block as a polynomial, the first bit in the block, i.e. frame 0, bit 1 or frame 8, bit 1, should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder.

Note 2 - There may be a need to update CRC-4 bits at intermediate equipment which access the S_{a4} bit message-based data-link (see § 2.3.4.5).

2.3.5.2 Encoding procedure

i) The CRC-4 bits in the SMF are replaced by binary 0s.

ii) The SMF is then acted upon by the multiplication/division process referred to in § 2.3.5.1.

iii) The remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

Note - The CRC-4 bits thus generated do not affect the result of the multiplication/division process in the next SMF because, as indicated in i) above, the CRC-4 bit positions in an SMF are initially set to 0 during the multiplication/division process.

2.3.5.3 Decoding procedure

i) A received SMF is acted upon by the multiplication/division process referred to in § 2.3.5.1, after having its CRC-4 bits extracted and replaced by 0s.

ii) The remainder resulting from this division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder calculated in the decoder exactly corresponds to the CRC-4 bits received in the next SMF, it is assumed that the checked SMF is error free.

2.3.5.4 Updating procedure at intermediate path points in a message-based data-link application

The S_{a4} bit may be used as a message-based data-link within 2048 kbit/s paths [see Note 4, ii) to Table 5a/G.704]. Situations are envisaged where access to this data link could be required at points on the path between the true path termination points, e.g. reporting of error performance data from intermediate sites along the path. In such situations it is important that the logical path termination role of CRC-4 is not invalidated or impaired. Hence, any changes to the S_{a4} bits within a SMF at an intermediate path point does not imply a recalculation of the CRC-$ bits over the whole SMF, but rather their update as a linear recoding function in respect of specific deterministic binary changes of the S_{a4} bits only.

Annex C to Recommendation G.706 gives further information regarding this updating procedure.

3 CHARACTERISTICS OF FRAME STRUCTURES CARRYING CHANNELS AT VARIOUS BIT RATES IN 2048 kbit/s (ITU-T Recommendation G.704 § 5 Mar 1994)

3.1 INTERFACE AT 2048 kbit/s CARRYING 64 kbit/s CHANNELS

3.1.1 Frame structure

3.1.1.1 Number of bits per 64 kbit/s channel time slot

Eight, numbered 1 to 8.

3.1.1.2 Number of 64 kbit/s channel time slots per frame

Bits 1 to 256 in the basic frame carry 32 octet interleaved time slots numbered 0 to 31.

3.1.1.3 Allocation of the bits of 64 kbit/s channel time slot 0

See Table 2.1 (see § 2.2).

3.1.2 Use of other 64 kbit/s channel time slots

Each of the 64 kbit/s channel time slots 1 to 15 and 17 to 31 can accommodate e.g., a PCM-encoded voiceband signal according to ITU-T Rec G.711 or a 64 kbit/s digital signal.

The 64 kbit/s channel time slot 16 may be used for signalling. If not needed for signalling, in some cases it may be used for a 64 kbit/s channel in the same way as time slots 1 to 15 and 17 to 31.

3.1.3 Signalling

The use of 64 kbit/s channel time slot 16 is recommended for either common channel or channel associated signalling as required.

The detailed requirements for the organisation of particular signalling systems will be included in the specifications for those signalling systems.

3.1.3.1 Common channel signalling

The 64 kbit/s channel time slot 16 may be used for common channel signalling systems up to a rate of 64 kbit/s. The method of obtaining signal alignment will form part of the particular common channel signalling specification.

3.1.3.2 Channel associated signalling

This section contains the recommended arrangement for the use of the 64 kbit/s capability of channel time slot 16 for channel associated signalling.

3.1.3.2.1 Multiframe structure

A multiframe comprises 16 consecutive frames (whose structure is given in § 3.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of 64 kbit/s channel time slot 16 in frame 0.

3.1.3.2.2 Allocation of 64-kbit/s channel time slot 16

When 64 kbit/s channel time slot 16 is used for channel associated signalling, the 64-kbit/s capacity is sub-multiplexed into lower-rate signalling channels using the multiframe alignment signal as a reference.

Details of the bit allocation are given in Table 3.1.

Table 3.1 : Bit allocation of channel associated 64 kbit/s time slot 16 for channel associated signalling (Table 9/G.704)

Time slot 16 of frame 0	Time slot 16 of frame 1		Time slot 16 of frame 2		---	Time slot 16 of frame 15	
0000xyxx	abcd channel 1	abcd channel 16	abcd channel 2	abcd channel 17	---	abcd channel 15	abcd channel 30

Note 1 - Channel numbers refer to telephone channel numbers. 64 kbit/s channel time slots 1 to 15 and 17 to 31 are assigned to telephone channel numbered from 1 to 30.

Note 2 - This bit allocation provides four 500 bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± 2 ms.

Note 3 - When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1. Bit b is used in Singapore, and its value is not fixed.

It is recommended that the combination 0000 of bits a, b, c and d should not be used for signalling purposes for channels 1-15.

Note 4 - x = spare bit, to be set to 1 if not used.
y = bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

3.2 INTERFACE AT 2048 kbit/s CARRYING N x 64 kbit/s

Electrical characteristics should follow PART B (see Note 4 of § 1). For the accommodation of n x 64 kbit/s time slots in the 2048 kbit/s frame, two situations are envisaged.

3.2.1 One n x 64 kbit/s signal on the tributary side of a multiple equipment

Time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2;

TS16: reserved for the accommodation, if required, of a 64 kbit/s signalling channel.

- If $2 \leq n \leq 15$, TS1 to TSn are filled with n x 64 kbit/s data [see a) of Figure 3.1];
- If $15 < n \leq 30$, TS1 to TS15 and TS17 to TS(n+l) are filled with n x 64 kbit/s data [see b) of Figure 3.1].
- Remaining time slots are filled with all 1s.

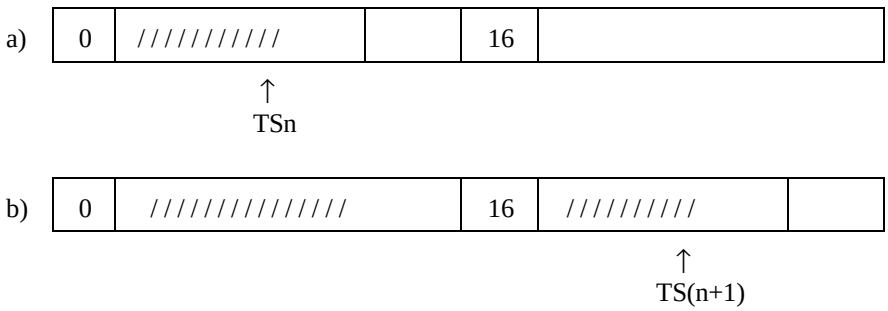

Figure 3.1 (Figure 1/G.704)

3.2.2 One or more n x 64 kbit/s signal on the multiplexed signal side of multiplexing equipment

For any one n x 64 kbit/s signal, time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2;

TS16: reserved for the accommodation, if required, of a 64 kbit/s signalling channel.

TS(x) of the 2048 kbit/s frame is designated as the time slot into which the first time slot of the n x 64 kbit/s is accommodated.

- If $x \leq 15$ and $x + (n-l) \leq 15$, or, if $x \geq 17$ and $x + (n-l) \leq 31$, then the filling of time slots is from TS(x) to TS (x+n-l) [see a) and b) of Figure 3.2];
- If $x + (n-l) \geq 16$, then the filling of time slots is from TS(x) to TS15 and TS17 to TS (x+n) [see c) of Figure 3.2].

Note - Once n x 64 kbit/s signal has been accommodated into the multiplexed signal, care should be taken in the interpretation of the above rules to ensure that further such signals only use the time slots which remain spare.

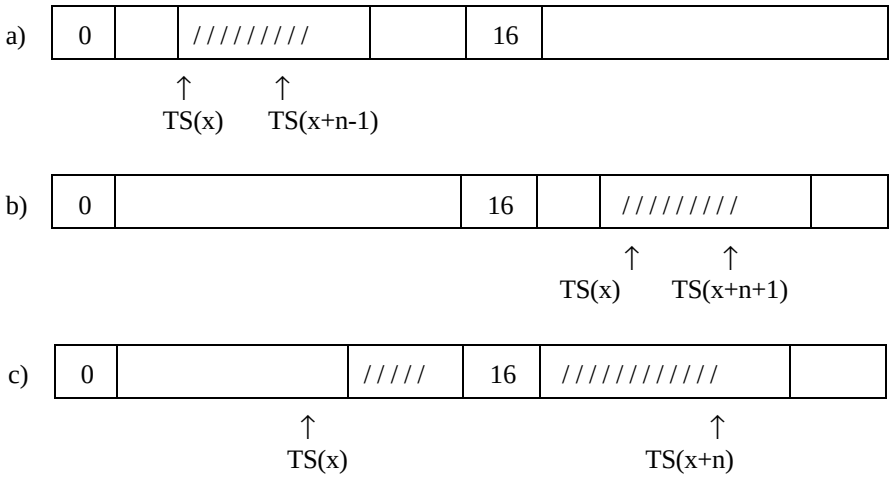

Figure 3.2 (Figure 2/G.704)